

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

Figure 2

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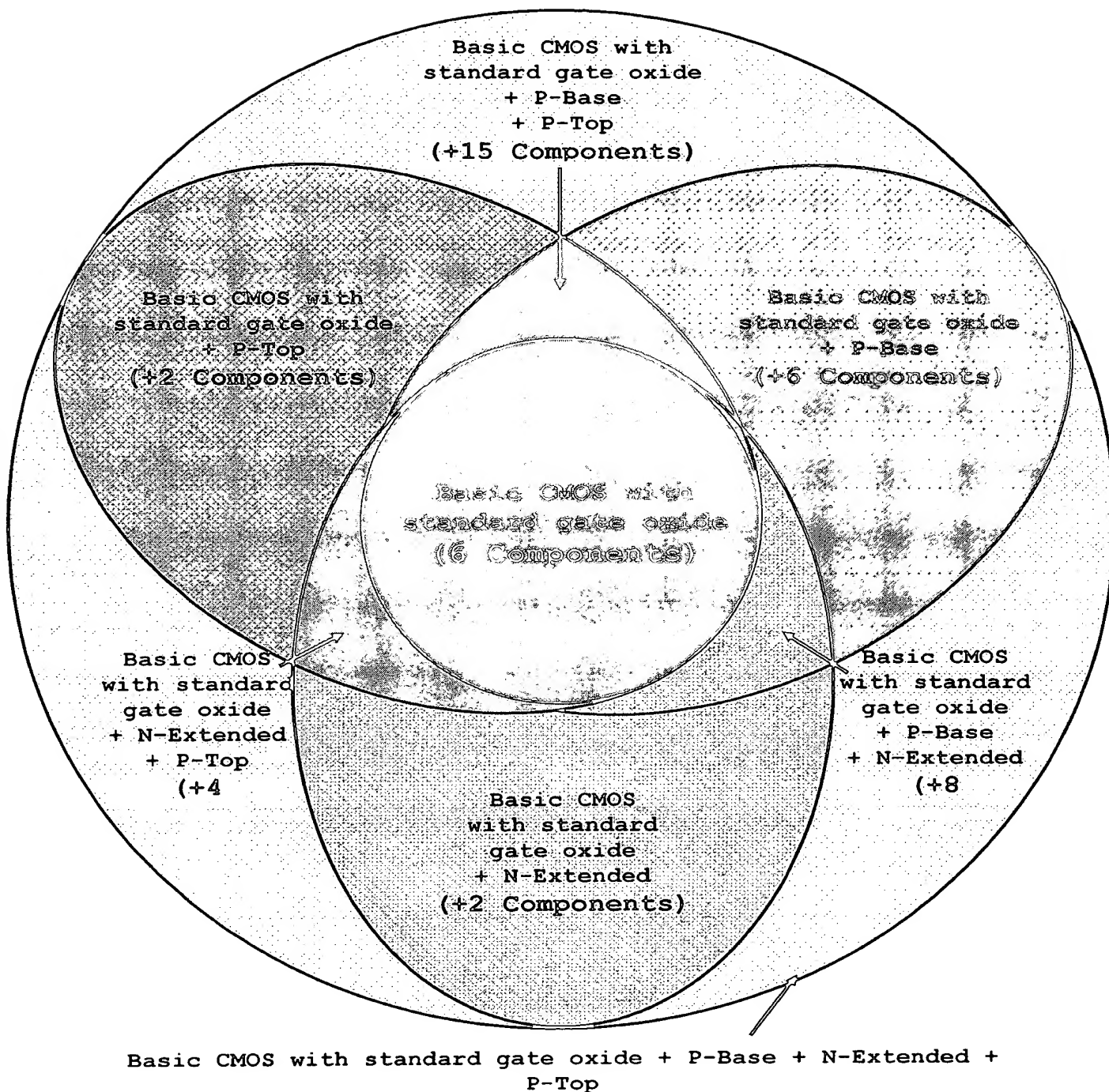


Figure 3

Name of Photolithographic Mask	Process Steps
Mask 1: N-Well	Starting Material : P- Bulk Silicon
	Oxidation (Initial oxide)
	Photo
	N-Type Implant (N-Well)
	Diffusion
Mask 2: Active Area	Oxide Etch
	Oxidation (Subnitox)
	Silicon Nitride Deposition (CVD)
	Photo
	Nitride Etch
Mask 3: P-Field	Photo
	P-Type Implant (P-Field)
	Blanket N-Type Implant (N-Field)
	Oxidation (Field Oxide)
	Nitride Etch
Mask 5: Thin Gate oxide & VTP Adjust	Oxide Etch
	Oxidation (Pre-Gate Oxide)
	Oxide Etch
	Oxidation (Thin Gate Oxide)
	Photo
Mask 6: Polysilicon Gate Patterning	P-Type Implant (VTP Adjust)
	Polysilicon Gate Deposition (CVD)
	Polysilicon Doping
	Photo
	Polysilicon Etch
Mask 8: N-Extended	Photo
Mask 10: N+ Implant	N-Type Implant (N-Extended)
	Oxidation and Diffusion
	Polysilicon Oxidation
	Photo
	N-Type Implant (N+)
Mask 11: P+ Implant	Photo
	P-Type Implant (P+)
	SG/PSG/SOG (Oxide) Deposition
	Diffusion
	Photo
Mask 12: Contacts	Contact Etch
	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
Mask 13: Metal 1	Dielectric and SOG (Oxide) Deposition
	Photo
	Vias Etch
	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
Mask 14: Vias	Photo
	Metal Etch
	Oxide / Nitride Deposition
	Photo
	Oxide Etch
Mask 15: Metal 2	
Mask 16: Passivation	

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

Name of Photolithographic Mask	Process Steps
Mask 1: N-Well	Starting Material : P- Bulk Silicon
	Oxidation (Initial oxide)
	Photo
	N-Type Implant (N-Well)
Mask 2: Active Area	Diffusion
	Oxide Etch
	Oxidation (Subnitox)
	Silicon Nitride Deposition (CVD)
Mask 3: P-Field	Photo
	Nitride Etch
	P-Type Implant (P-Field)
	Blanket N-Type Implant (N-Field)
	Oxidation (Field Oxide)
	Nitride Etch
	Oxide Etch
	Oxidation (Pre-Gate Oxide)
Mask 5: Thin Gate oxide & VTP Adjust	Oxide Etch
	Oxidation (Thin Gate Oxide)
	Photo
Mask 6: Polysilicon Gate Patterning	P-Type Implant (VTP Adjust)
	Polysilicon Gate Deposition (CVD)
	Polysilicon Doping
	Photo
Mask 9: P-Top	Polysilicon Etch
	Photo
Mask 10: N+ Implant	P-Type Implant (P-Top)
	Oxidation and Diffusion
	Polysilicon Oxidation
	Photo
Mask 11: P+ Implant	N-Type Implant (N+)
	Photo
	P-Type Implant (P+)
Mask 12: Contacts	SG/PSG/SOG (Oxide) Deposition
	Diffusion
	Photo
	Contact Etch
Mask 13: Metal 1	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
	Dielectric and SOG (Oxide) Deposition
Mask 14: Vias	Photo
	Vias Etch
Mask 15: Metal 2	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
	Oxide / Nitride Deposition
Mask 16: Passivation	Photo
	Oxide Etch

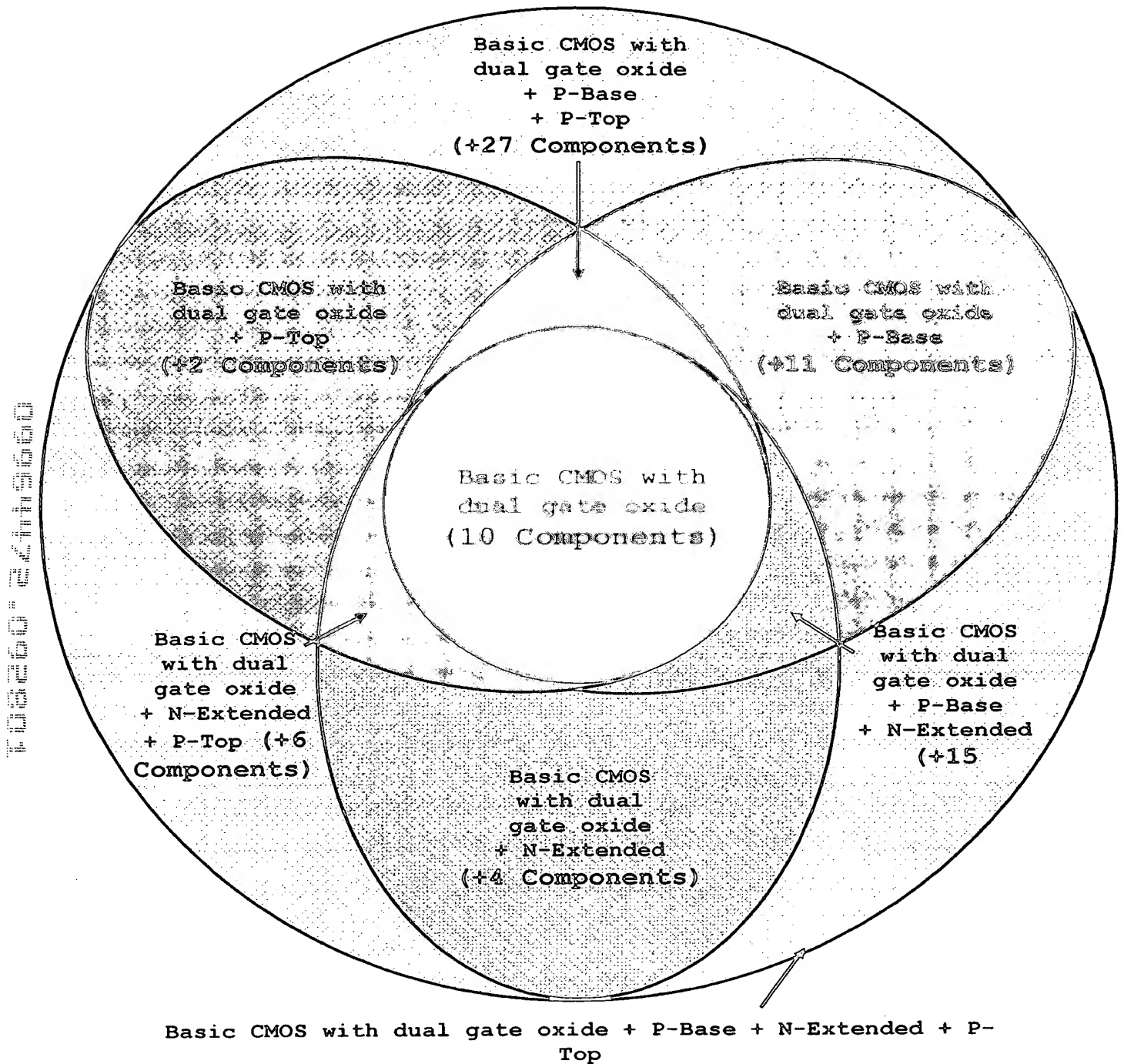
[illegible]

Figure 8

Name of Photolithographic Mask	Process Steps
Mask 1: N-Well	Starting Material : P- Bulk Silicon
	Oxidation (Initial oxide)
	Photo
	N-Type Implant (N-Well)
	Diffusion
Mask 2: Active Area	Oxide Etch
	Oxidation (Subnitox)
	Silicon Nitride Deposition (CVD)
	Photo
	Nitride Etch
Mask 3: P-Field	Photo
	P-Type Implant (P-Field)
	Blanket N-Type Implant (N-Field)
	Oxidation (Field Oxide)
	Nitride Etch
	Oxide Etch
Mask 5: Thin Gate oxide & VTP Adjust	Oxidation (Pre-Gate Oxide)
	Oxide Etch
	Oxidation (Thin Gate Oxide)
	Photo
	P-Type Implant (VTP Adjust)
Mask 6: Polysilicon Gate Patterning	Polysilicon Gate Deposition (CVD)
	Polysilicon Doping
	Photo
	Polysilicon Etch
Mask 7: P-Base	Photo
	P-Type Implant (P-Base)
Mask 9: P-Top	Photo
	P-Type Implant (P-Top)
Mask 10: N+ Implant	Oxidation and Diffusion
	Polysilicon Oxidation
	Photo
	N-Type Implant (N+)
Mask 11: P+ Implant	Photo
	P-Type Implant (P+)
Mask 12: Contacts	SG/PSG/SOG (Oxide) Deposition
	Diffusion
	Photo
	Contact Etch
Mask 13: Metal 1	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
	Dielectric and SOG (Oxide) Deposition
Mask 14: Vias	Photo
	Vias Etch
Mask 15: Metal 2	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
	Oxide / Nitride Deposition
Mask 16: Passivation	Photo
	Oxide Etch

700000-22113000

Figure 10



[illegible]

Name of Photolithographic Mask	Process Steps
Mask 1: N-Well	Starting Material : P- Bulk Silicon
	Oxidation (Initial oxide)
	Photo
	N-Type Implant (N-Well)
Mask 2: Active Area	Diffusion
	Oxide Etch
	Oxidation (Subnitox)
	Silicon Nitride Deposition (CVD)
Mask 3: P-Field	Photo
	Nitride Etch
	Photo
	P-Type Implant (P-Field)
	Blanket N-Type Implant (N-Field)
	Oxidation (Field Oxide)
	Nitride Etch
	Oxide Etch
Mask 4: High-voltage Gate Oxide	Oxidation (Pre-Gate Oxide)
	Oxide Etch
	Oxidation (High-voltage Gate Oxide)
Mask 5: Thin Gate oxide & VTP Adjust	Photo
	Oxide Etch
	Oxidation (Thin Gate Oxide)
	Photo
Mask 6: Polysilicon Gate Patterning	P-Type Implant (VTP Adjust)
	Polysilicon Gate Deposition (CVD)
	Polysilicon Doping
	Photo
	Polysilicon Etch
Mask 9: P-Top	Photo
Mask 10: N+ Implant	P-Type Implant (P-Top)
	Oxidation and Diffusion
	Polysilicon Oxidation
Mask 11: P+ Implant	Photo
	N-Type Implant (N+)
	Photo
Mask 12: Contacts	P-Type Implant (P+)
	SG/PSG/SOG (Oxide) Deposition
	Diffusion
	Photo
	Contact Etch
Mask 13: Metal 1	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
	Dielectric and SOG (Oxide) Deposition
Mask 14: Vias	Photo
	Vias Etch
Mask 15: Metal 2	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
	Oxide / Nitride Deposition
Mask 16: Passivation	Photo
	Oxide Etch

Figure 14

Name of Photolithographic Mask	Process Steps
Mask 1: N-Well	Starting Material : P- Bulk Silicon
	Oxidation (Initial oxide)
	Photo
	N-Type Implant (N-Well)
	Diffusion
Mask 2: Active Area	Oxide Etch
	Oxidation (Subnitox)
	Silicon Nitride Deposition (CVD)
	Photo
	Nitride Etch
Mask 3: P-Field	Photo
	P-Type Implant (P-Field)
	Blanket N-Type Implant (N-Field)
	Oxidation (Field Oxide)
	Nitride Etch
	Oxide Etch
	Oxidation (Pre-Gate Oxide)
Mask 4: High-voltage Gate Oxide	Oxide Etch
Mask 5: Thin Gate oxide & VTP Adjust	Oxidation (High-voltage Gate Oxide)
	Photo
	Oxide Etch
	Oxidation (Thin Gate Oxide)
Mask 6: Polysilicon Gate Patterning	Photo
	P-Type Implant (VTP Adjust)
	Polysilicon Gate Deposition (CVD)
	Polysilicon Doping
	Photo
Mask 8: N-Extended	Polysilicon Etch
	Photo
Mask 9: P-Top	N-Type Implant (N-Extended)
	Photo
Mask 10: N+ Implant	P-Type Implant (P-Top)
	Oxidation and Diffusion
	Polysilicon Oxidation
	Photo
Mask 11: P+ Implant	N-Type Implant (N+)
	Photo
	P-Type Implant (P+)
	SG/PSG/SOG (Oxide) Deposition
Mask 12: Contacts	Diffusion
	Photo
	Contact Etch
	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
Mask 13: Metal 1	Photo
	Metal Etch
	Dielectric and SOG (Oxide) Deposition
	Photo
Mask 14: Vias	Vias Etch
	Photo
Mask 15: Metal 2	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
Mask 16: Passivation	Oxide / Nitride Deposition
	Photo
	Oxide Etch

Figure 19a

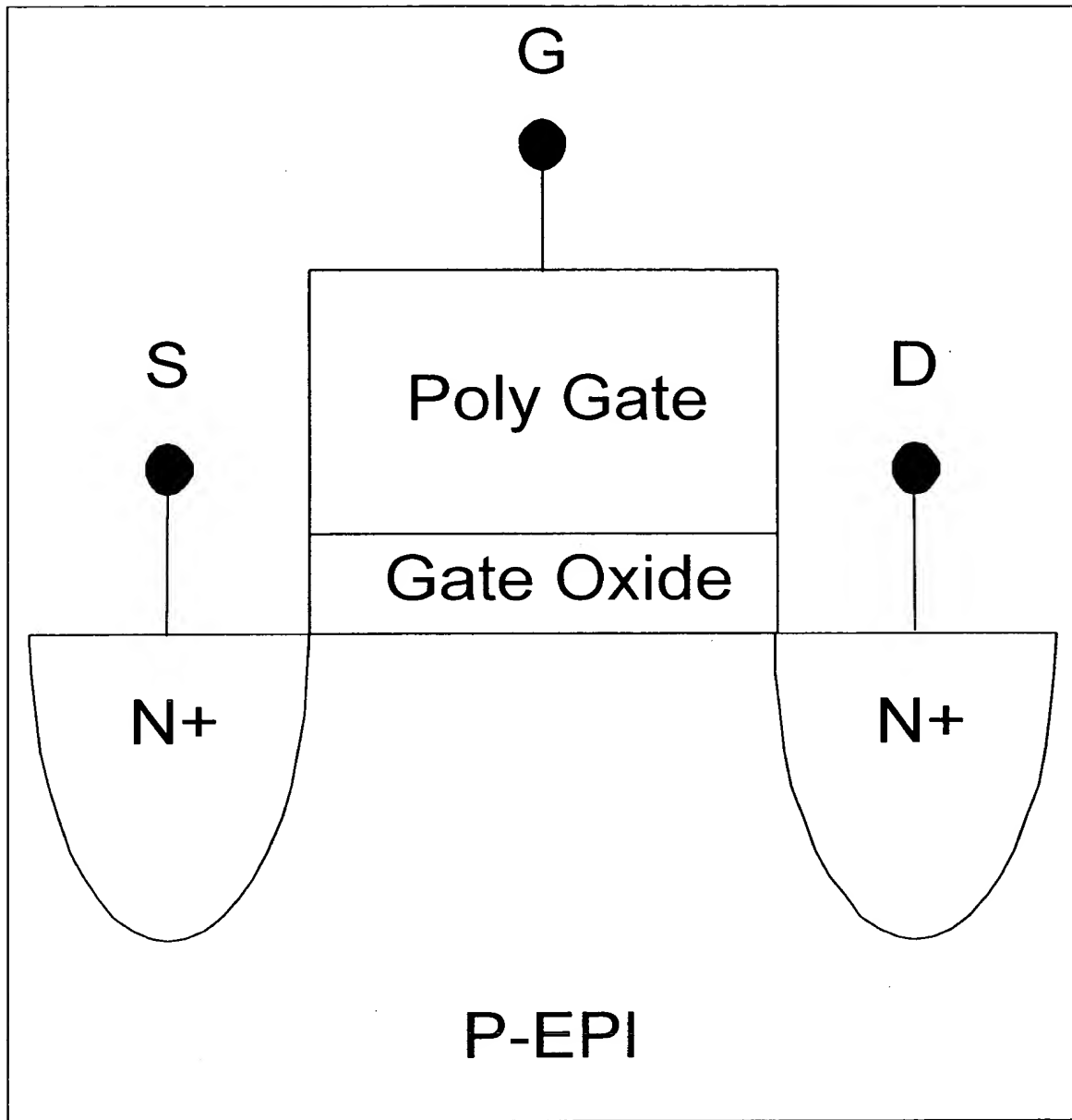
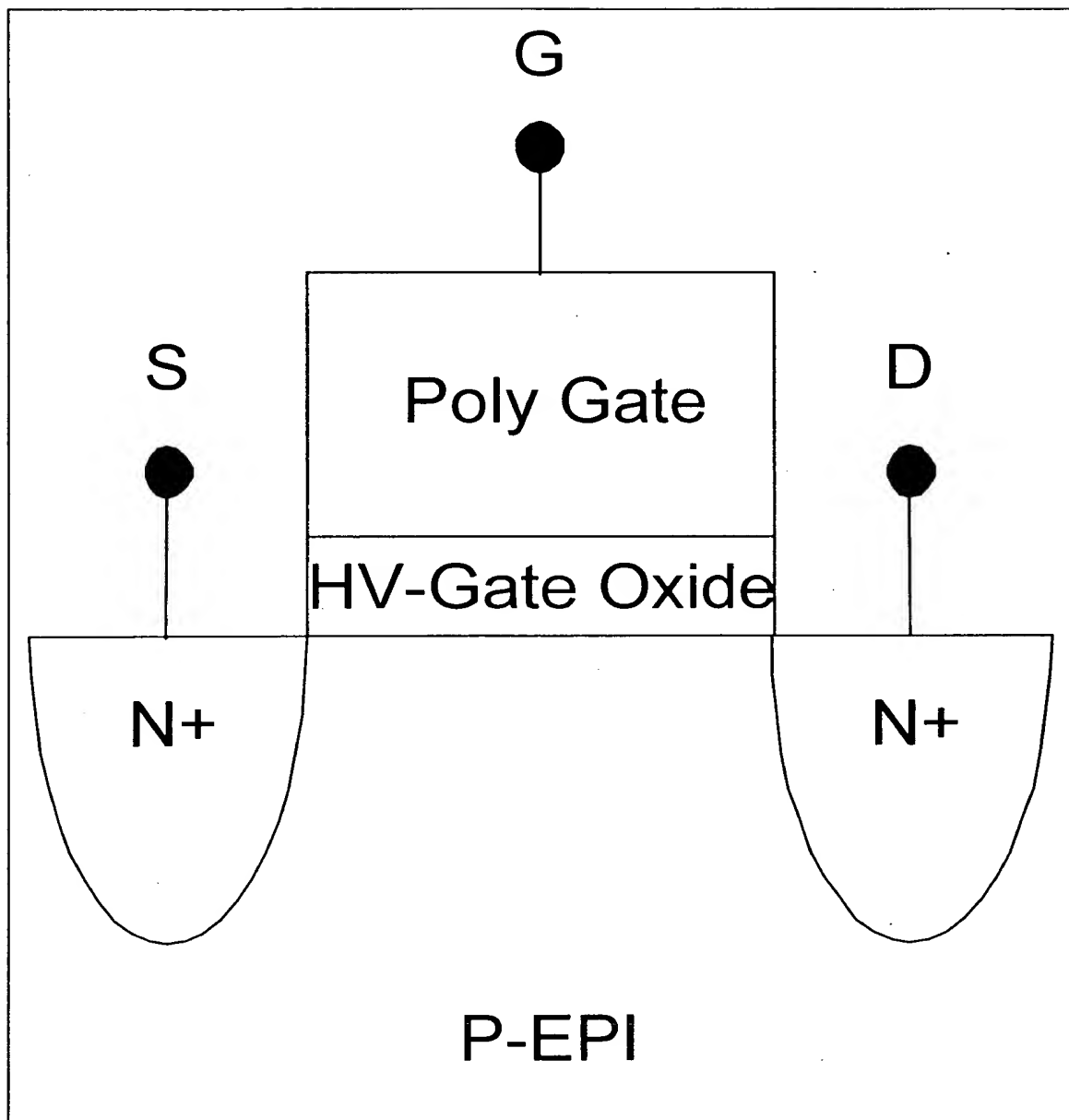


Figure 19b



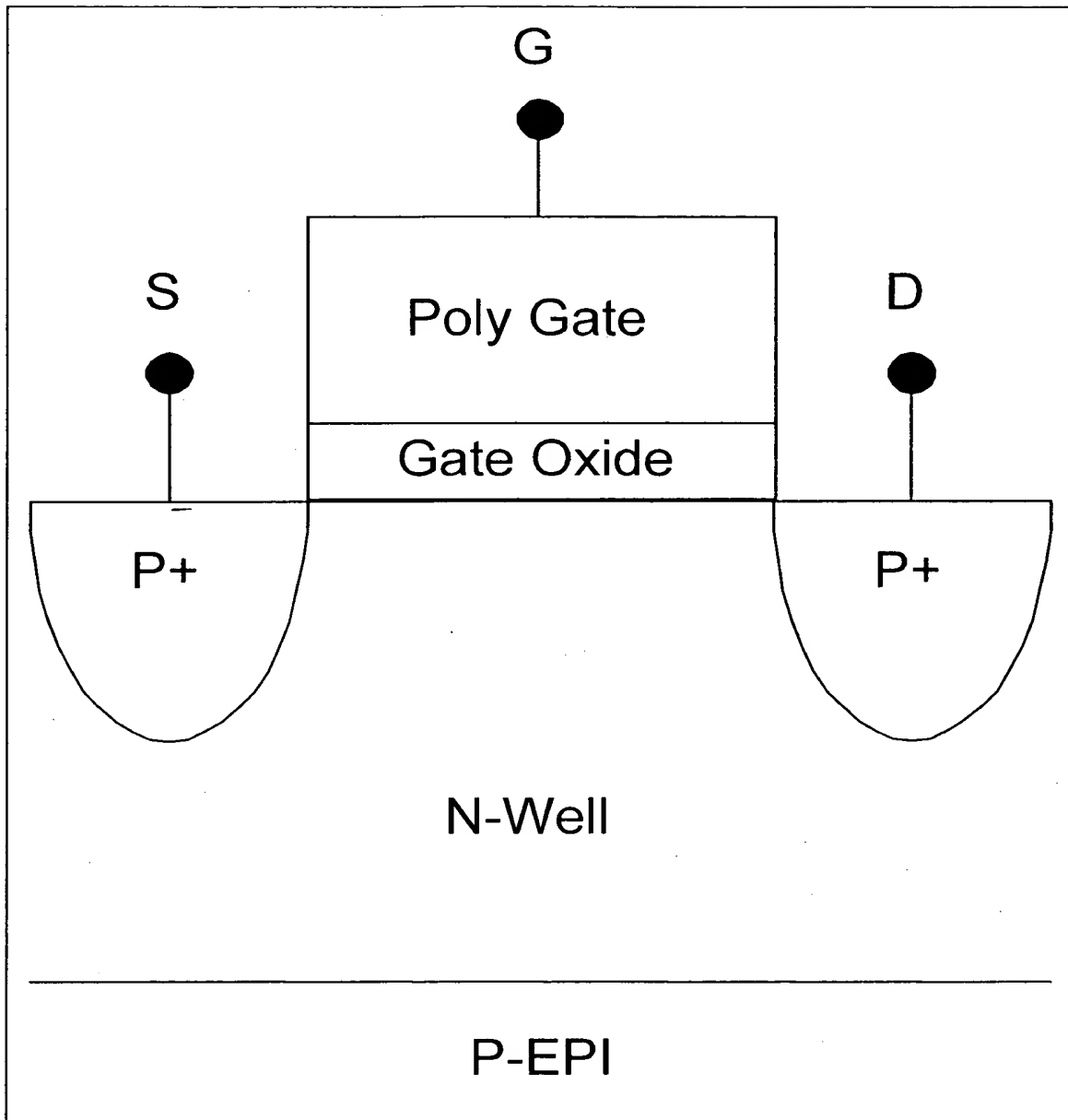
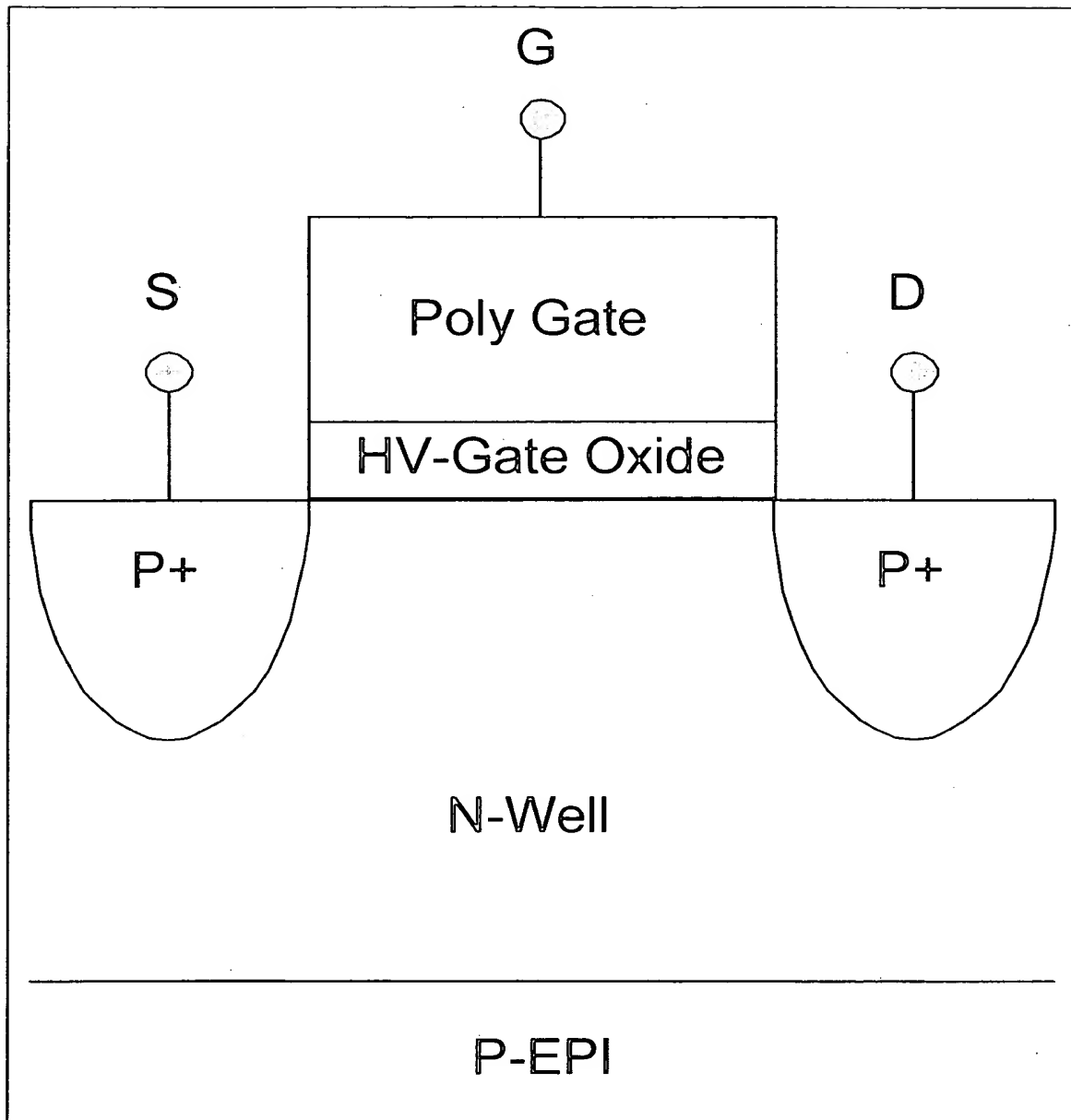
[illegible]

Figure 20b



108250" 2443660

Figure 21a

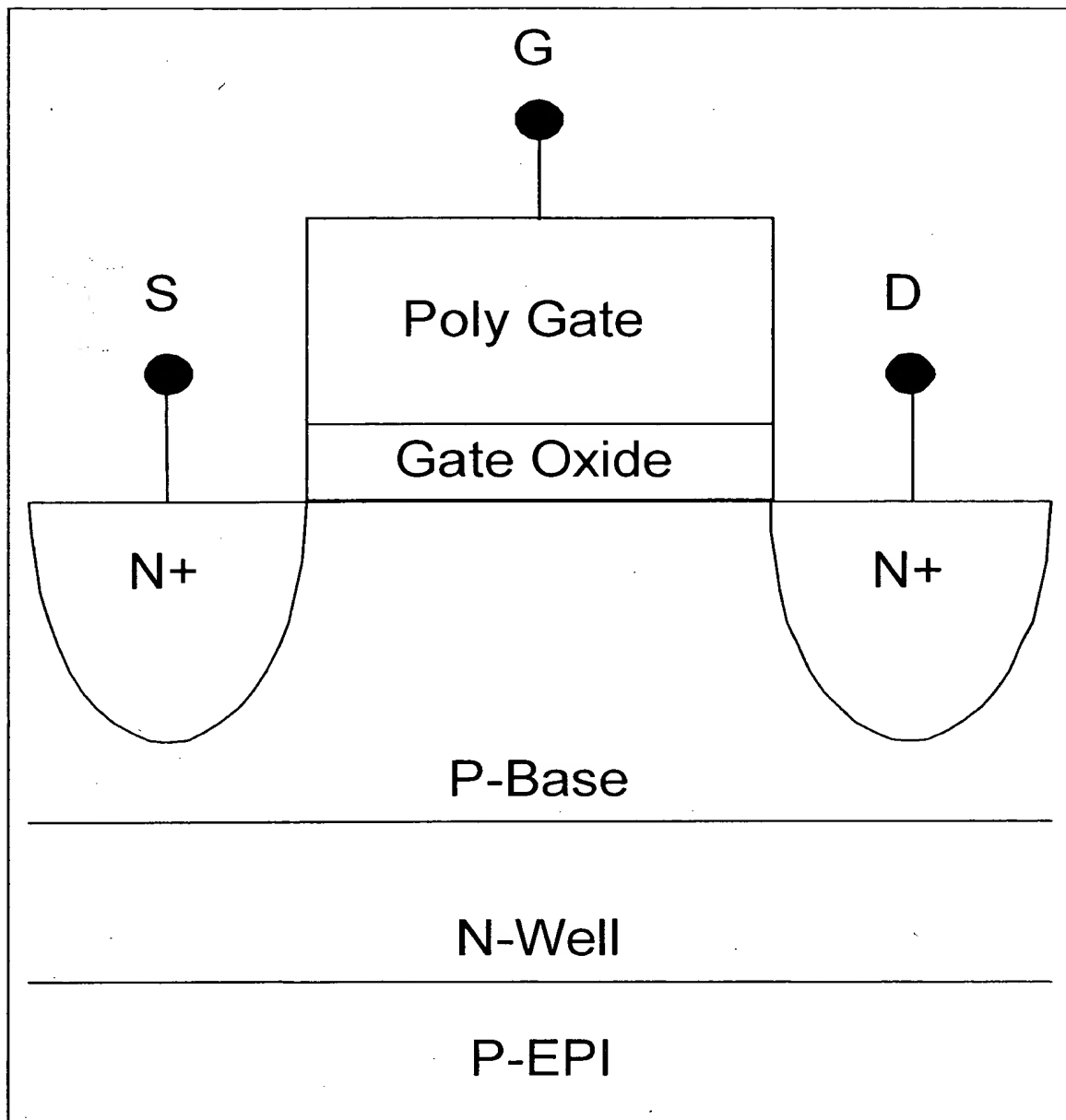
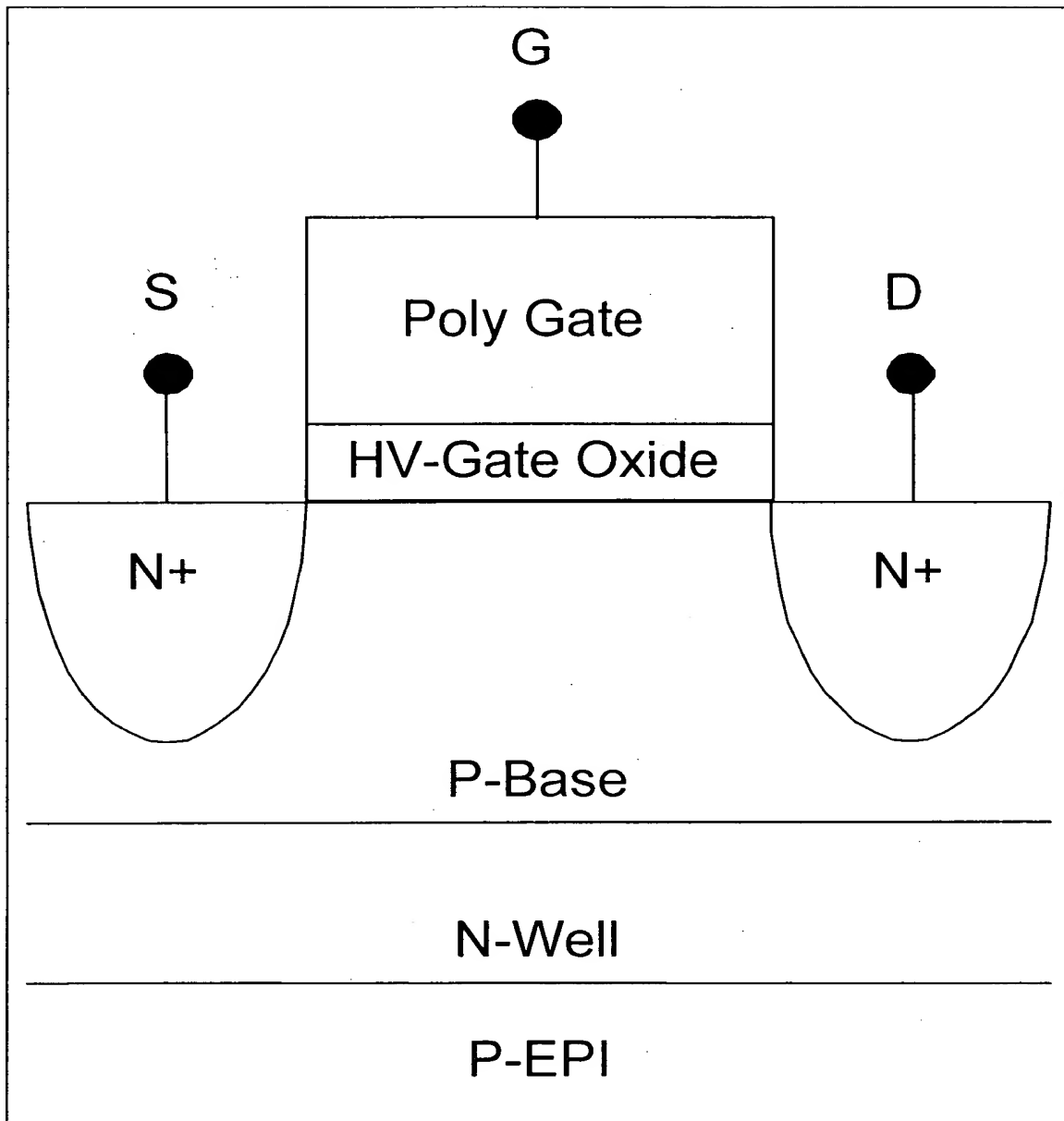


Figure 21a

Figure 21b



000000 2419600

Figure 22a

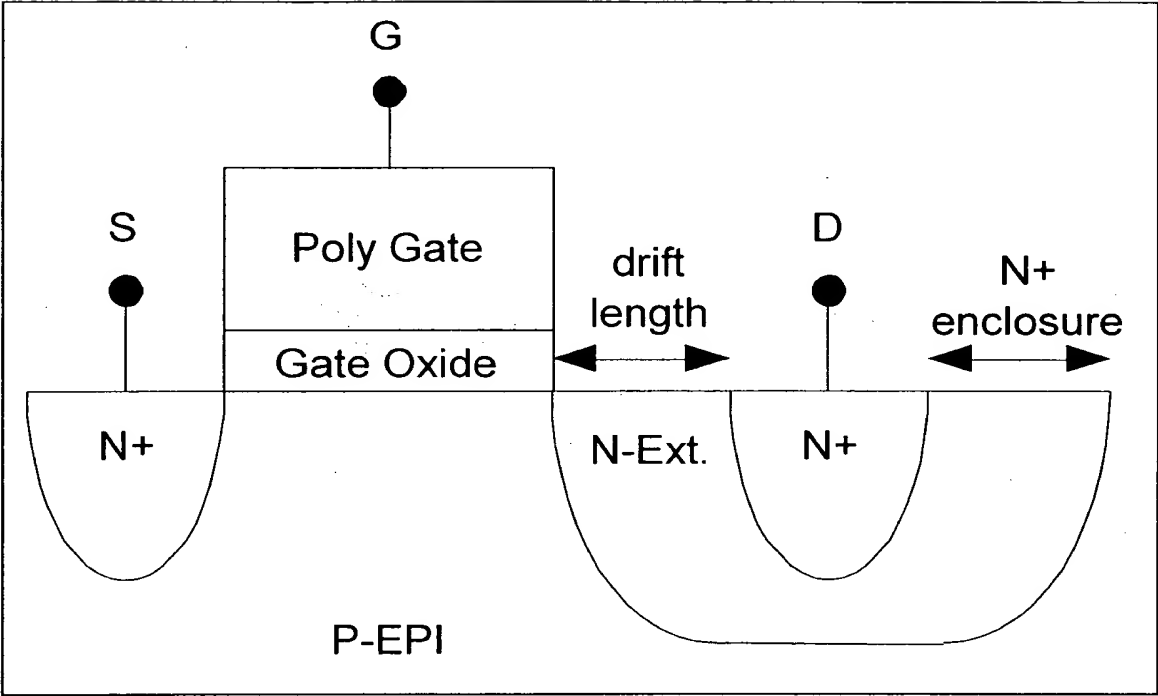
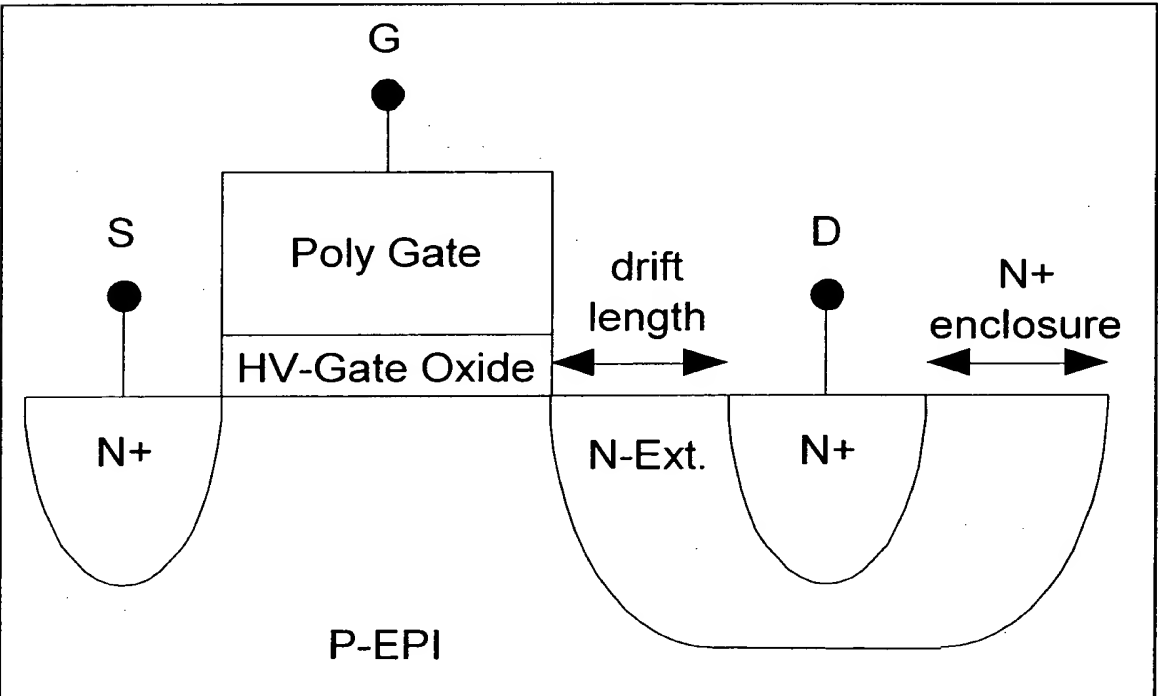
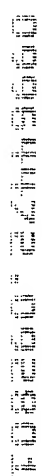
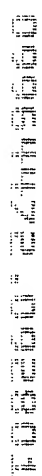


Figure 22b



[illegible][illegible]

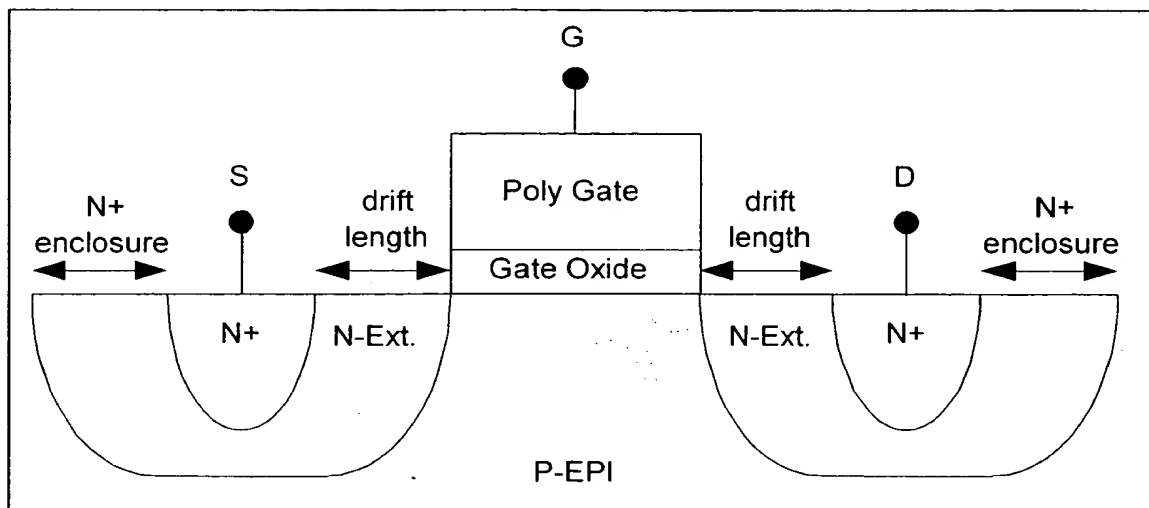
[illegible]

Figure 24b

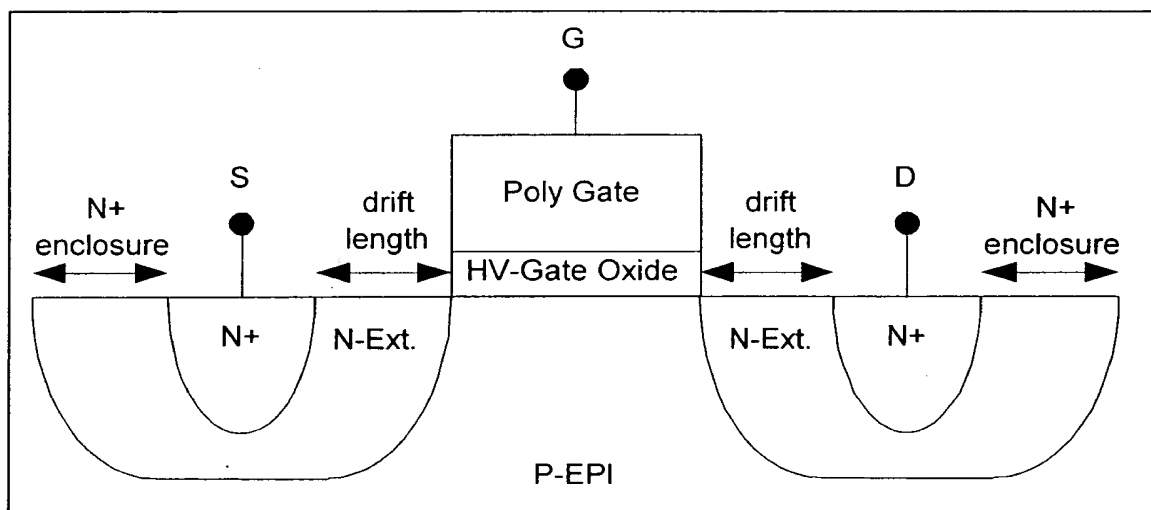


Figure 25a

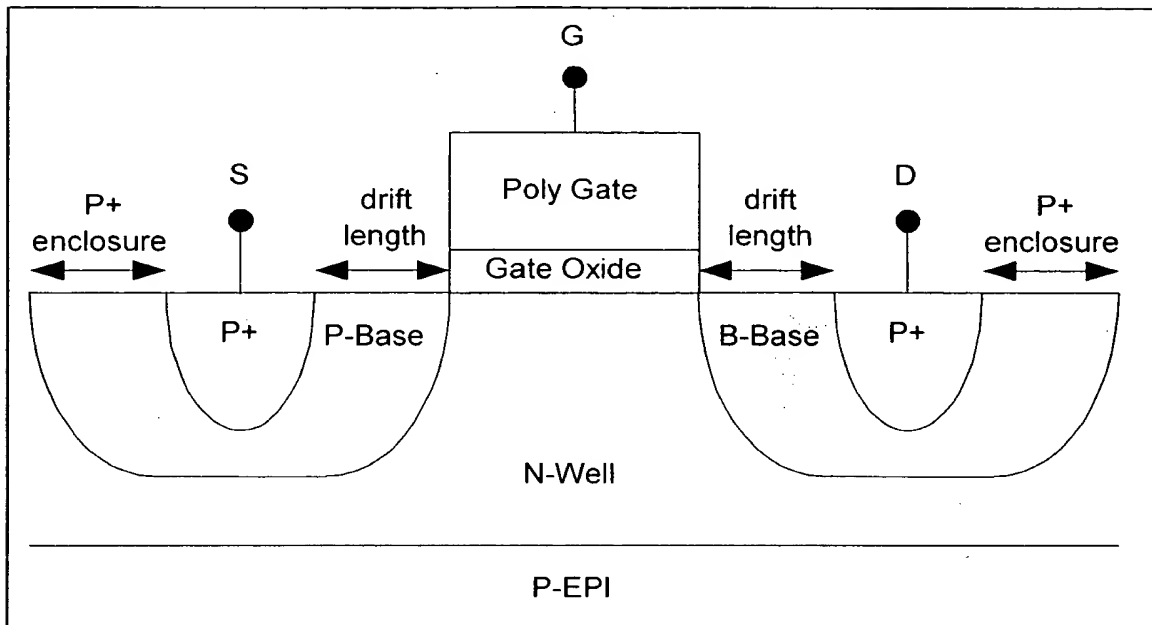
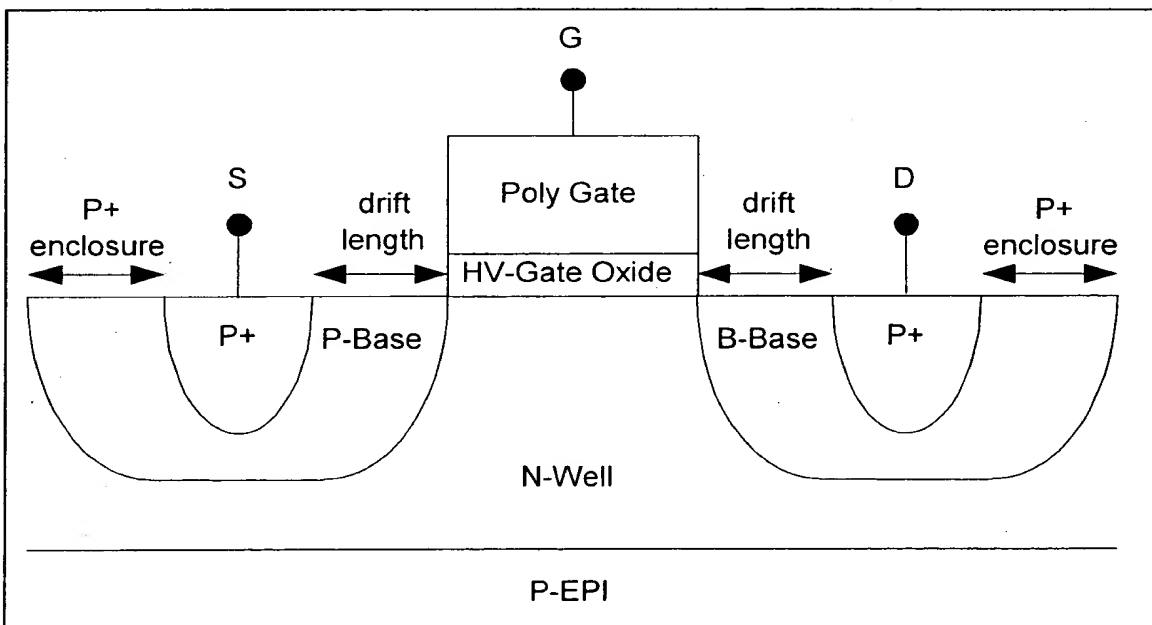


Figure 25b



100200 22113660

Figure 26a

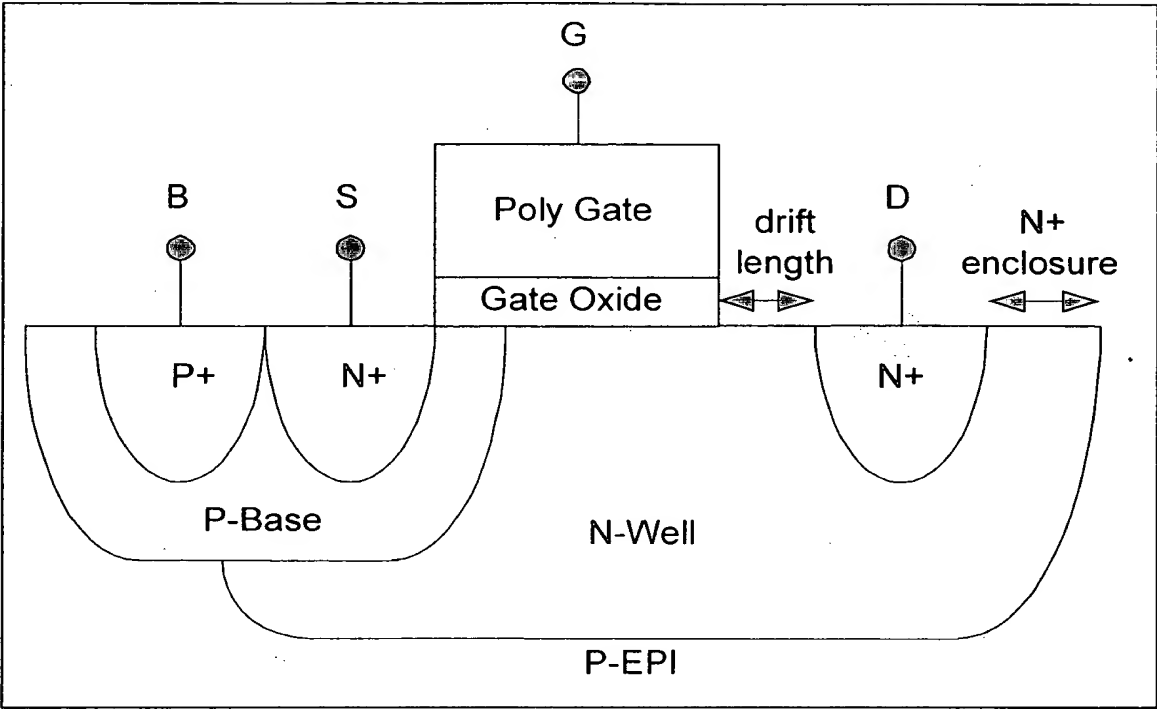


Figure 26b

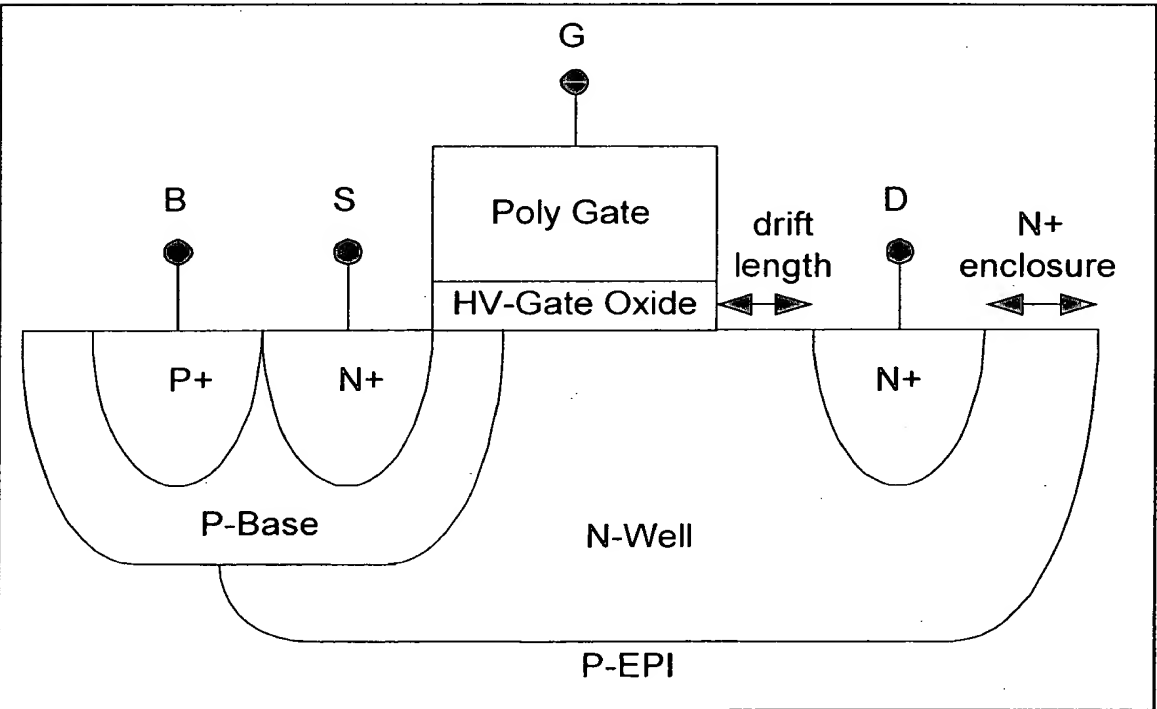


Figure 27a

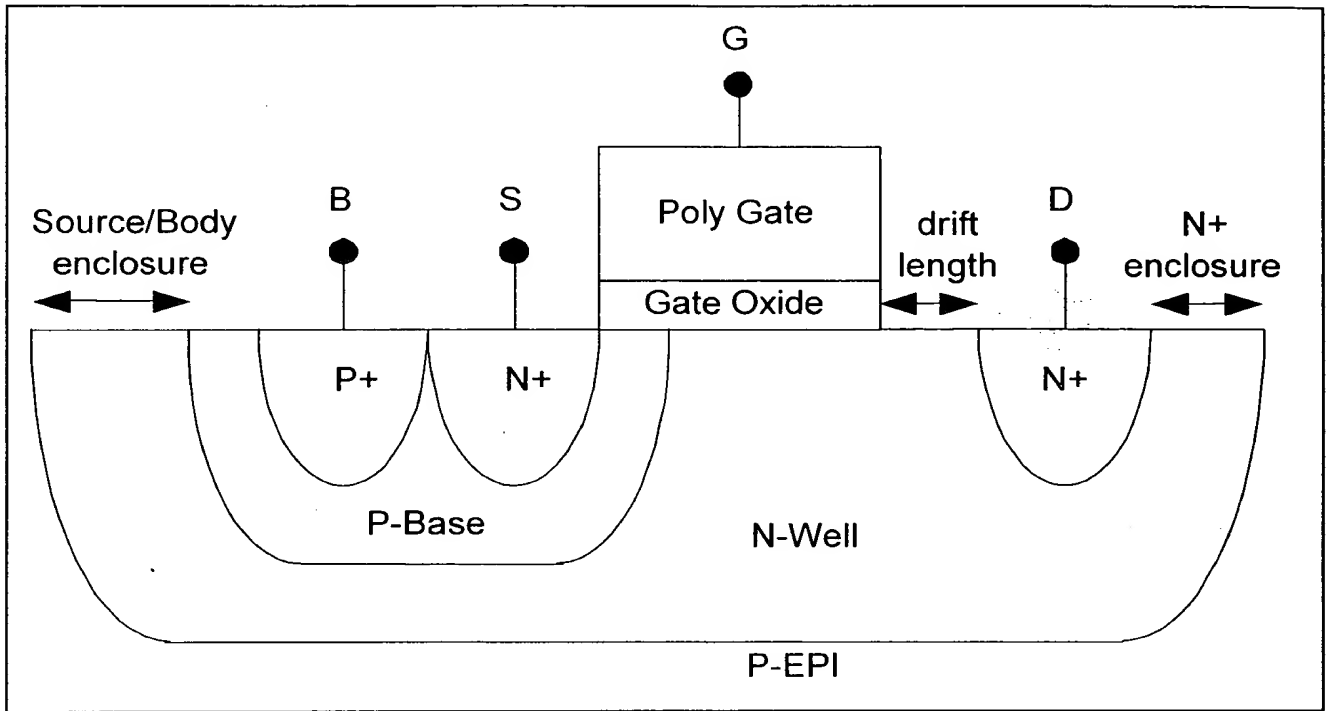


Figure 27b

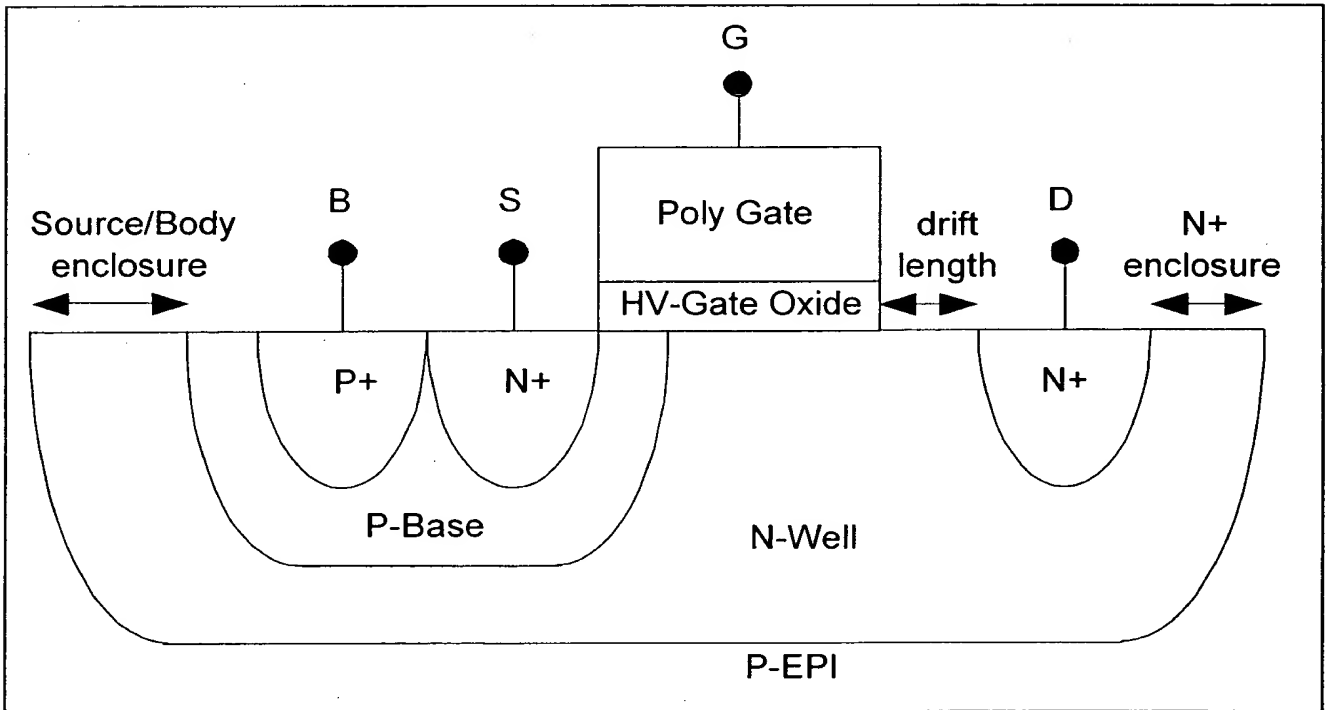


Figure 28a

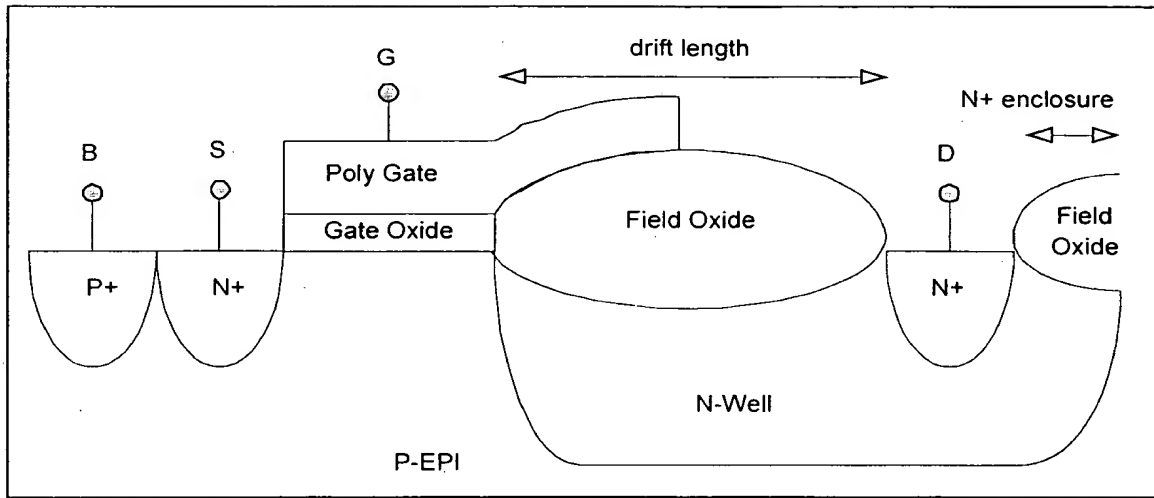


Figure 28b

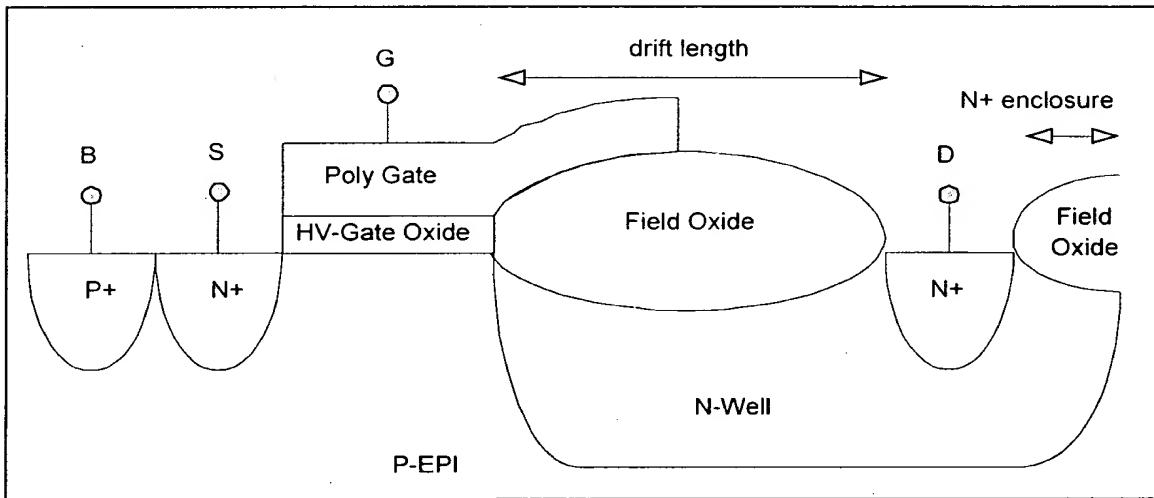


FIGURE 28a

Figure 29a

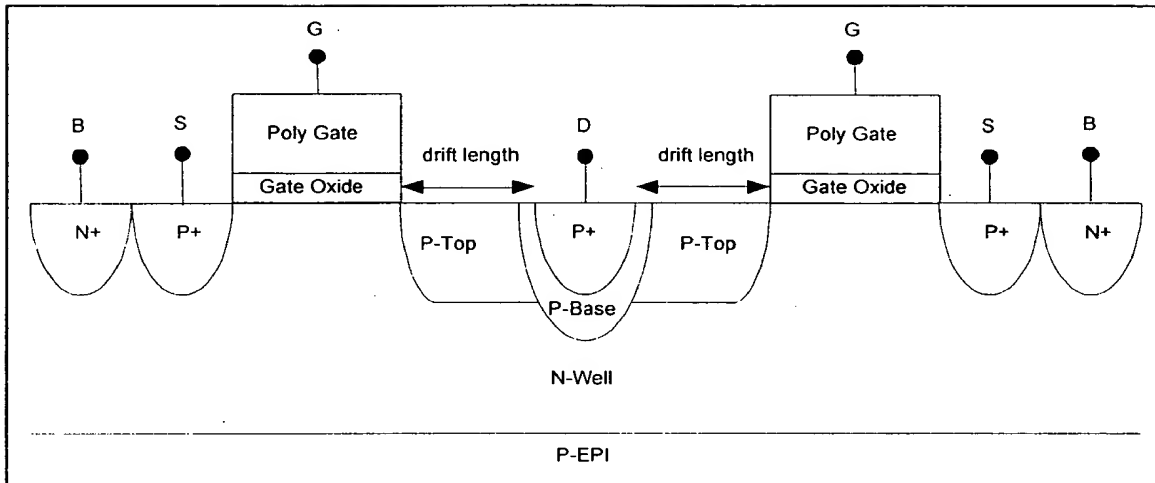


Figure 29b

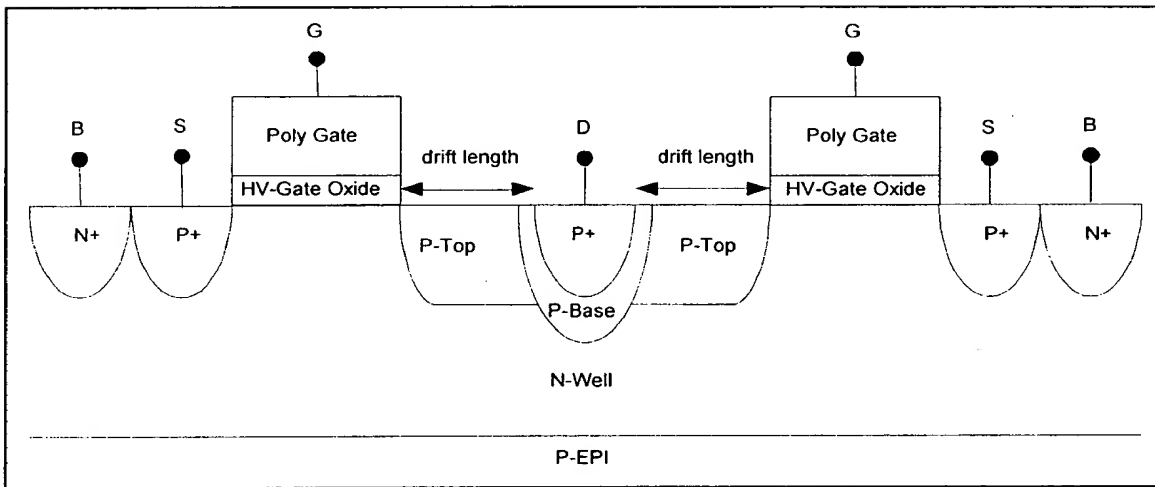


Figure 29a

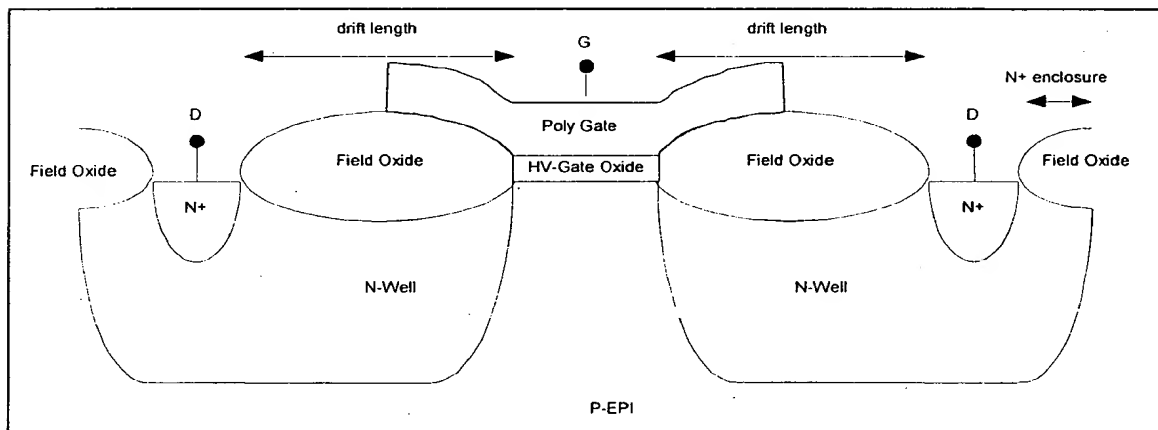
[illegible]

Figure 31a

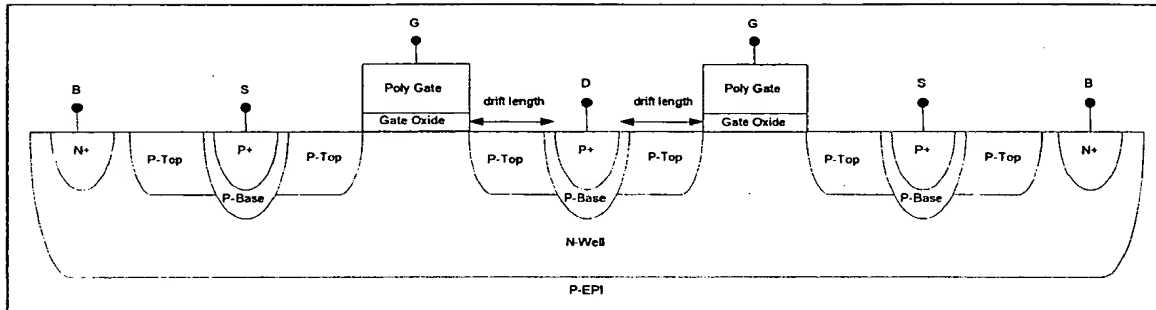


Figure 31b

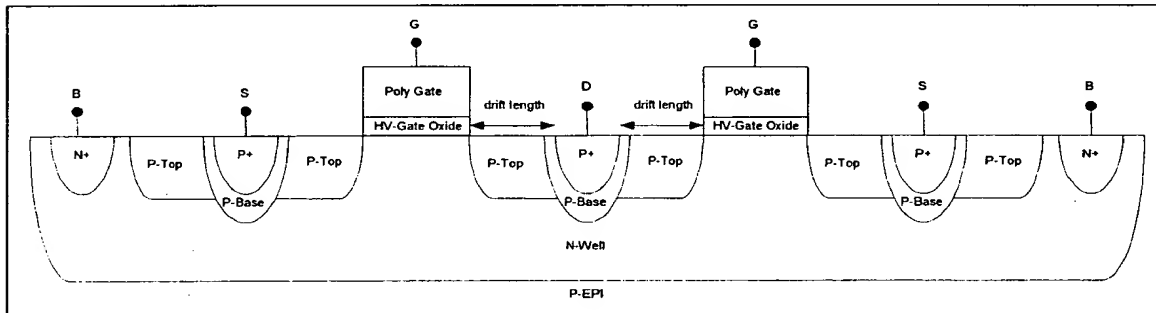


Figure 32a

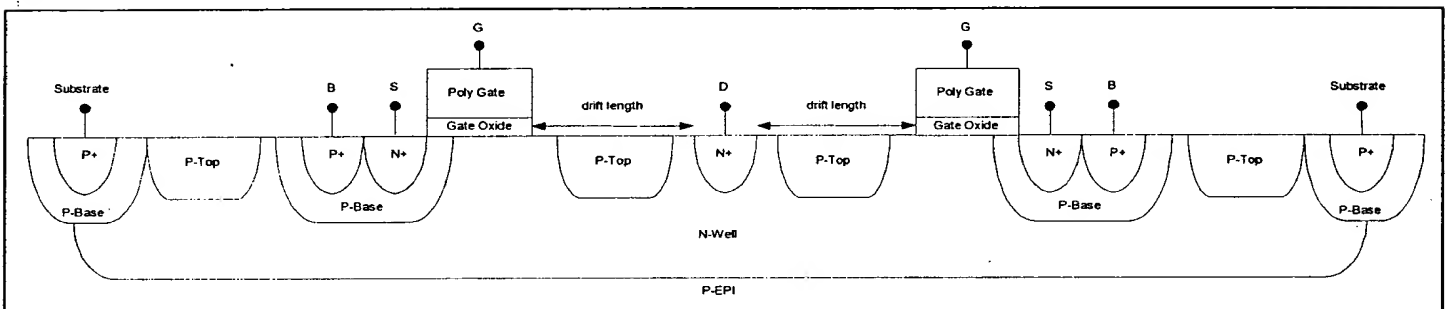


Figure 32b

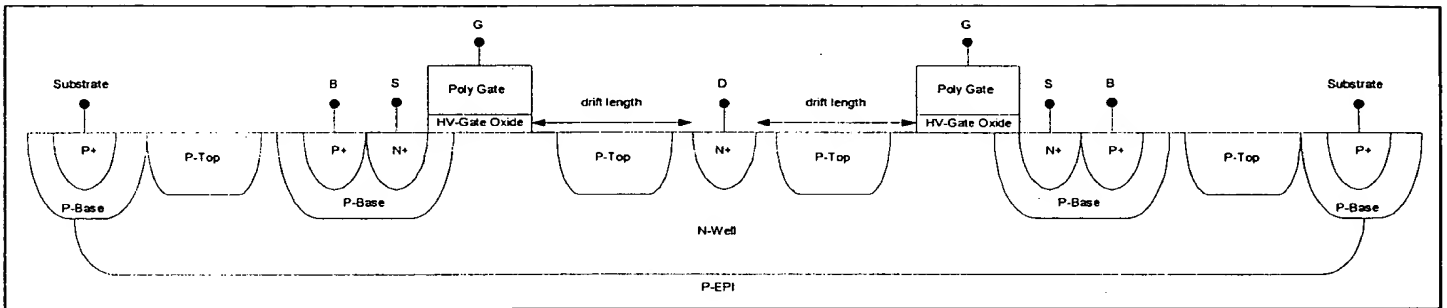


Figure 33a

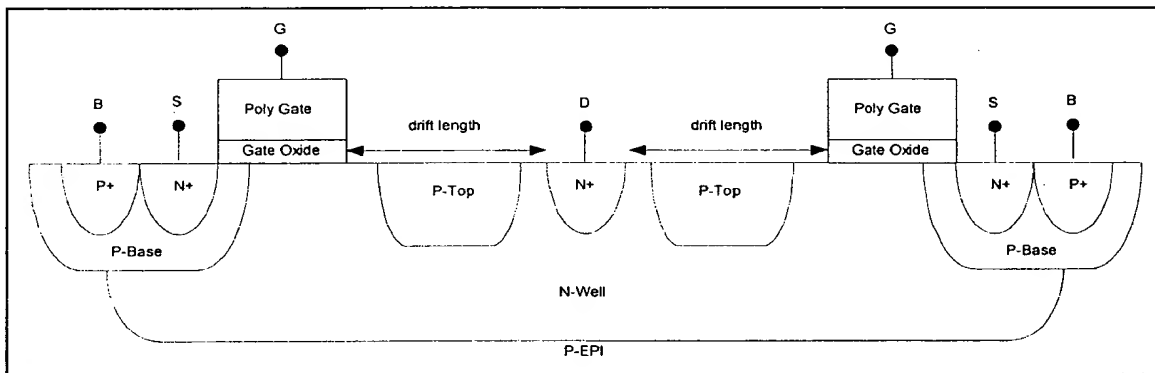


Figure 33b

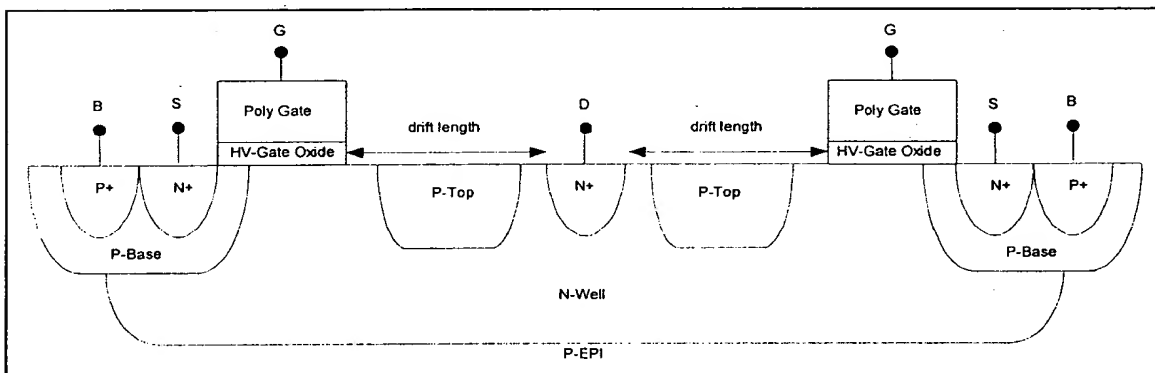


Figure 34a

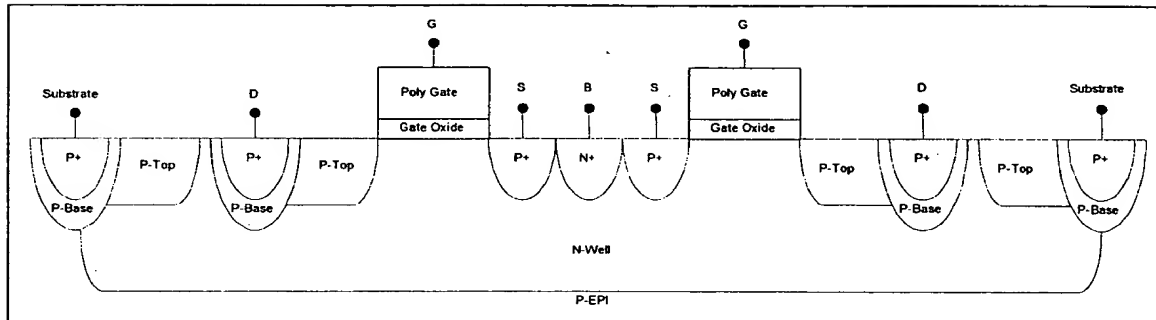


Figure 34b

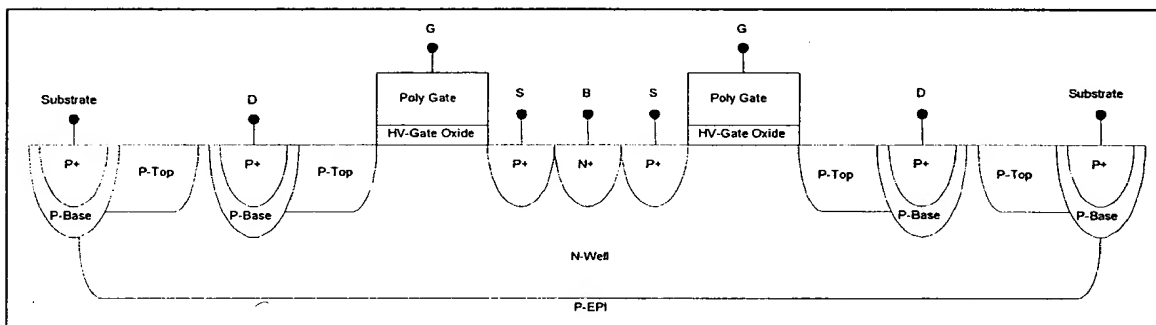


Figure 35a

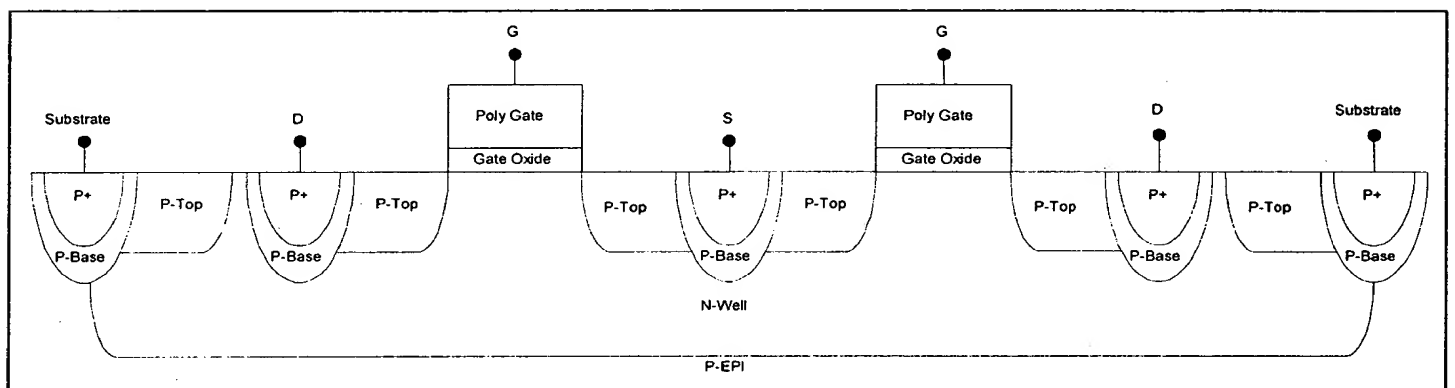


Figure 35b

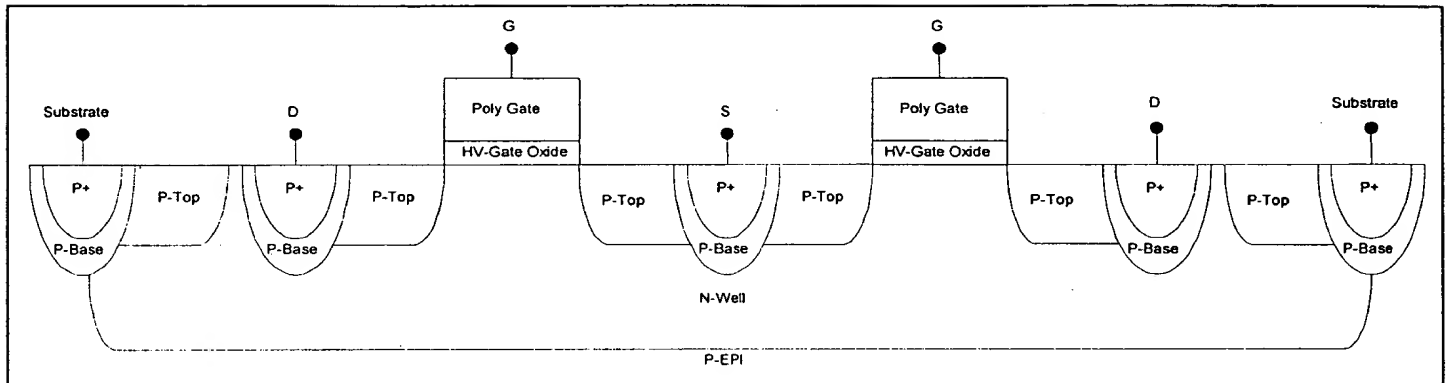


Figure 36

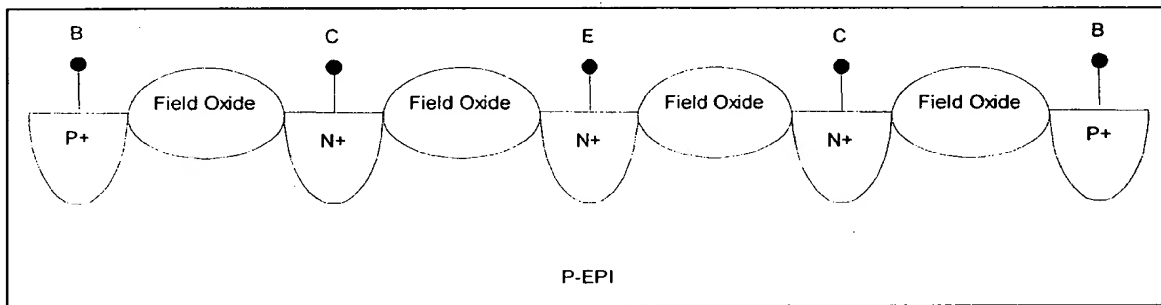


Figure 37

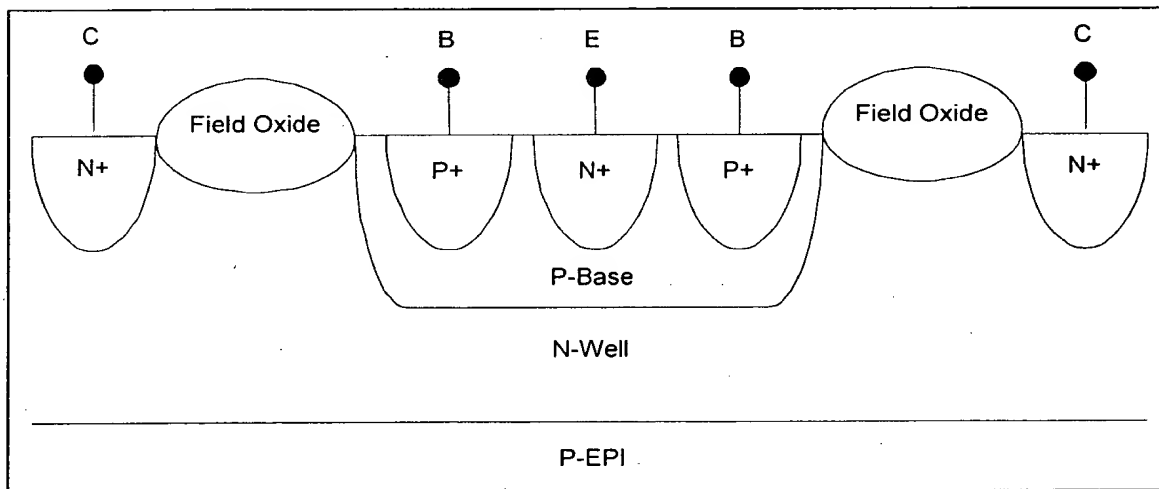


Figure 38

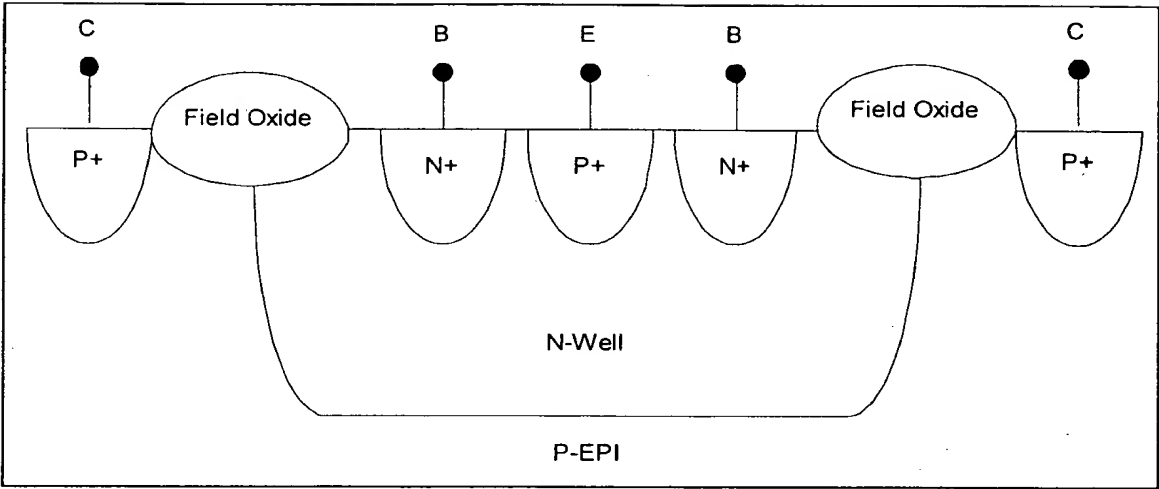


Figure 39

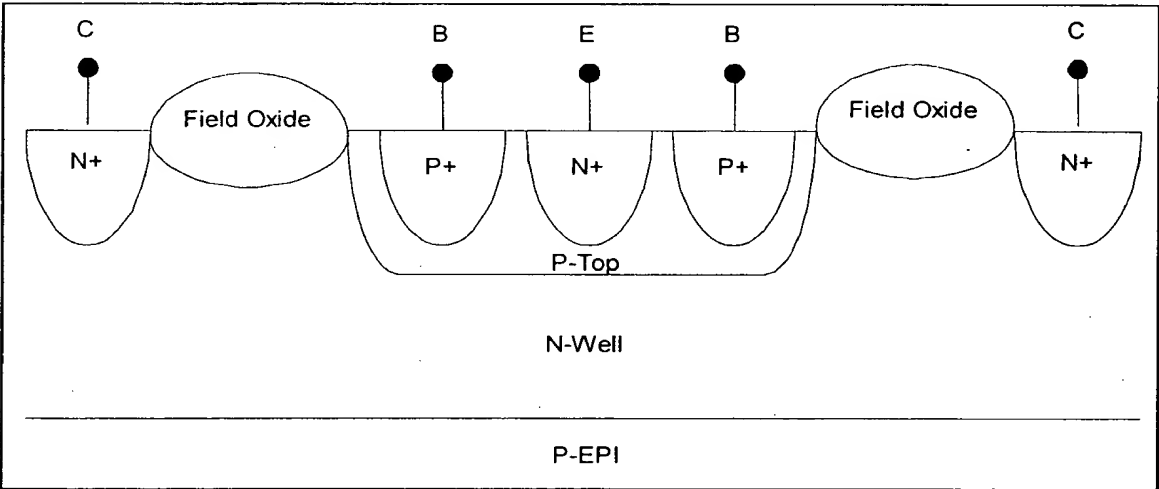


Figure 40

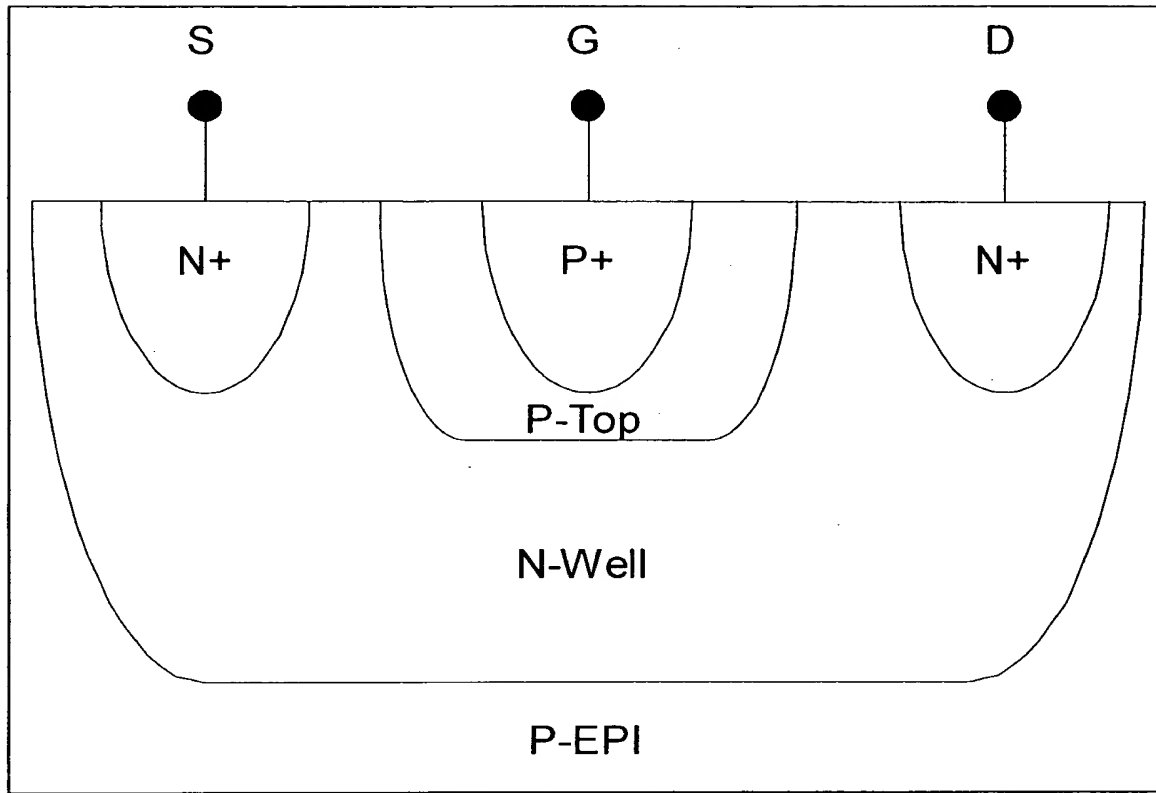


Figure 41a

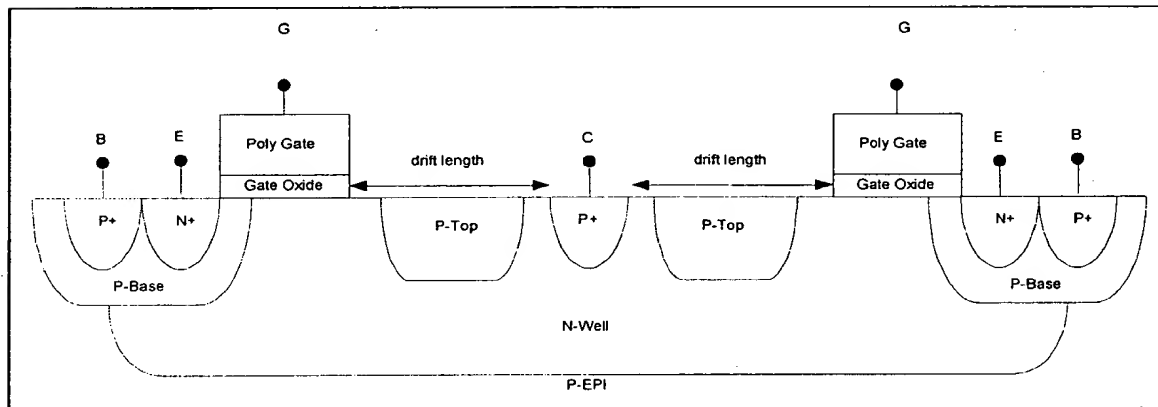


Figure 42

Active Component	Maximum	
	Gate Voltage (V)	Maximum Drain Voltage (V)
The standard N-MOSFET of Figure 19a	15	5.5
The standard N-MOSFET of Figure 19b	40	5.5
The standard P-MOSFET of Figure 20a	15	5.5
The standard P-MOSFET of Figure 20b	40	5.5
The standard Junction isolated N-MOSFET of Figure 21a	15	5.5
The standard Junction isolated N-MOSFET of Figure 21b	40	5.5
The mid-voltage single extended N-MOSFET of Figure 22a	15	40
The mid-voltage single extended N-MOSFET of Figure 22b	40	40
The mid-voltage single extended P-MOSFET of Figure 23a	15	40
The mid-voltage single extended P-MOSFET of Figure 23b	40	40
The mid-voltage double extended N-MOSFET of Figure 24a	15	40
The mid-voltage double extended N-MOSFET of Figure 24b	40	40
The mid-voltage double extended P-MOSFET of Figure 25a	15	40
The mid-voltage double extended P-MOSFET of Figure 25b	40	40
The mid-voltage single extended N-LDMOSFET of Figure 26a	15	75
The mid-voltage single extended N-LDMOSFET of Figure 26b	40	75
The mid-voltage floating source N-LDMOSFET of Figure 27a	15	75
The mid-voltage floating source N-LDMOSFET of Figure 27b	40	75
The high-voltage single extended N-MOSFET of Figure 28a	15	
100		
The high-voltage single extended N-MOSFET of Figure 28b	40	
100		
The high-voltage single extended P-MOSFET of Figure 29a	15	
100		
The high-voltage single extended P-MOSFET of Figure 29b	40	
100		
The high-voltage double extended N-MOSFET of Figure 30a	15	
100		
The high-voltage double extended N-MOSFET of Figure 30b	40	
100		
The high-voltage double extended P-MOSFET of Figure 31a	15	
100		
The high-voltage double extended P-MOSFET of Figure 31b	40	
100		
The high-voltage double extended N-LDMOSFET of Figure 32a	15	
325		
The high-voltage double extended N-LDMOSFET of Figure 32b	40	
325		
The very-high-voltage single extended N-LDMOSFET of Figure 33a	15	
600		
The very-high-voltage single extended N-LDMOSFET of Figure 33b	40	
600		
The very-high-voltage single extended P-MOSFET of Figure 34a	15	
325		
The very-high-voltage single extended P-MOSFET of Figure 34b	40	
325		
The very-high-voltage double extended P-MOSFET of Figure 35a	15	
325		

FIGURE 42

Figure 43

Junction	Typical Sheet Resistance	Typical Breakdown Voltage
P+ / N-Well	65 Ohms/sq.	20 Volts
N+ / P-Substrate	50 Ohms/sq.	25 Volts
P-Top / N-Well	14 kOhms/sq.	40 Volts
P-Base / N-Well	1.75 kOhms/sq.	45 Volts
N-Ext. / P-Substrate	4 kOhms/sq.	45 Volts
N-Well / P-Substrate	1.5 kOhms/sq.	150 Volts
N-Well / P-Top / P-Substrate (RESURF)	-	650 Volts

[illegible]